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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/533,550	11/17/2005	Andrew Graham	1432.116.101/P29858	6310

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DICKE, BILLIG & CZAJA
FIFTH STREET TOWERS
100 SOUTH FIFTH STREET, SUITE 2250
MINNEAPOLIS, MN 55402

EXAMINER	
LOPEZ ESQUERRA, ANDRES	

ART UNIT	PAPER NUMBER
2818	

MAIL DATE	DELIVERY MODE
09/18/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/533,550	GRAHAM ET AL.	
	Examiner	Art Unit	
	ANDRES LOPEZ ESQUERRA	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-25,27-37 and 39-45* is/are pending in the application.

4a) Of the above claim(s) *43 and 45* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-25,27-37,39-42 and 44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Acknowledgement is made of Amendments filled July 22, 2008.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 22, 41, and 44 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

5. The new limitation to all independent claims of having "within each of the dielectric sublayers, a region in the via hole between the nanostructure and the respective dielectric sublayer been free of electrically insulating material" is not supported by the original specification of the application. Examiner would like to point out the process disclosed in the application does not clearly state what is or is not present in the via hole (108) between the nanostructure and the dielectric subalayers. For examination purposes the limitation will not be entered to the claims.

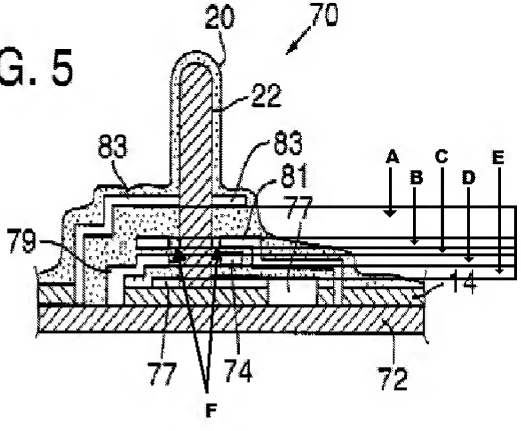
Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 22, 33 – 35, 40 – 41, and 44 are rejected under 35 U.S.C. 102(e) as being anticipated by Farnworth et al. US 6,515,325.

FIG. 5



8. As for claims 22, 41, and 44, Farnworth discloses (Col. 7, lines 29 – 38) and show sin Fig. 5 vertically integrated field-effect transistor comprising:

a. a first electrically conductive layer (77);

b. a middle layer (A, C, E), formed partially from dielectric material, on the first electrically conductive layer;

c. a second electrically conductive layer (83) on the middle layer;

d. and a nanostructure (22) integrated in a via hole introduced into the middle layer, the nanostructure further comprising a first end portion that is coupled to the first electrically conductive layer and a second end portion that is coupled to the second electrically conductive layer (Fig. 5),

e. wherein the middle layer, between two adjacent dielectric sublayers, has a third electrically conductive layer (B) , the thickness of which is less than the thickness of at least one of the dielectric sublayers(Fig. 5) (thickness of A is greater than B); and

f. wherein a ring structure (F) (the ring is formed from the insulation lager around the nanostructure) formed from an electrically insulating material as gate-insulating region of the field-effect transistor is arranged in the third electrically conductive layer, along the via hole that has been introduced therein,

g. wherein the middle layer has an additional electrically conductive layer (D), which at least one additional electrically conductive layer serves as an additional gate electrode of the field- effect transistor, with an additional ring structure formed from an electrically insulating material as an additional gate-

insulating region of the field-effect transistor being arranged along the via hole that has been introduced in the additional electrically conductive layer.

9. A recitation of "wherein the first end portion of the nanostructure forms a first source/drain region and the second end portion of the nanostructure forms a second source/drain region of the field-effect transistor" (Claim 22) and "for providing a gate-insulating region of the field effect transistor (Claims 22, 41, and 44) of the claimed invention does not result in a structural difference between the claimed invention and the prior art, thus claimed invention is only an art recognized suitability for an intended purpose, MPEP 2144.07

10. Also, as to the limitation of "formed from" (claims 22 and 44) and "wherein the ring-shaped means is formed from the third electrically conductive layer" (claim 41) are considered as a product by process limitations. "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even thought the prior product was made by a different process." In re Thorpe, 777F, 2d 659, 698, 227 USPQ 964, 966 (Fed. Cir. 1985); see also MPEP 2113.

11. As fro claims 33 – 35 and 40, Farnworth discloses (Col. 2, line 36, Col. 4, lines 22 – 31) the use of a carbon nanotube as the nanostructure and the use of polycrystalline for the substrate.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

14. Claims 22 – 25, 27 – 28, and 30 – 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mancevski US 2001/0023986 (Mancevski) in view of Choi et al US 2002/0001905 (Choi).

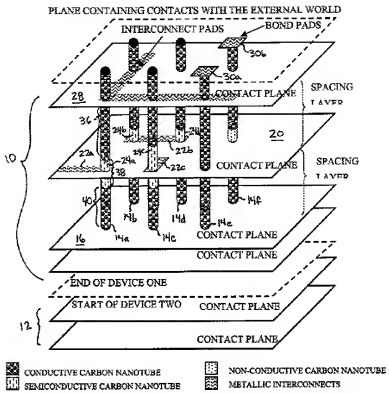


Figure 2

15. As for claims 22 and 41 – 43, Mancevski discloses (Page 3 [0040]) and shows in Fig. 2 a carbon nanotube transistor and method of manufacturing the same comprising:

h. a first electrically conductive layer (16);

i. a middle layer /spacing layers(10), formed partially from dielectric material, on the first electrically conductive layer;

j. a second electrically conductive layer on the middle layer (28), and;

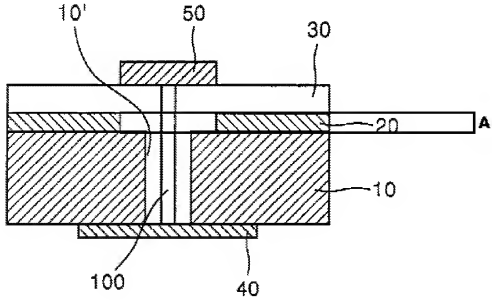
k. a nanostructure (14) integrated in a via hole/vertically aligned holes introduced into the middle layer, the nanostructure further comprising a first end portion that is coupled to the first electrically conductive layer and a second end

portion that is coupled to the second electrically conductive layer (as shown in the Fig, 2 both ends of the nanotubes are imbedded in the contact layer);

l. wherein the middle layer, between two adjacent dielectric sublayers/spacing layers, has a third electrically conductive layer (20), the thickness of which is less than the thickness of at least one of the dielectric sublayers (as shown in Fig 2, the contact plane is thinner than the spacing layers).

16. Mancevski fails to disclose use of a ring structure formed from an electrically insulating material as gate-insulating region of the field-effect transistor is arranged in the third electrically conductive layer, which forms the gate electrode of the field-effect transistor, along the via hole that has been introduced therein.

FIG. 1



17. Choi discloses (Page 2, [0028]) and shows in Fig. 1 a FET transistor and method of manufacturing the same comprising a nanostructure (100) and the use of an insulation ring (A) in the are of the gate (20) of the transistor.

18. Choi is evidence that ordinary workers in the art would find a reason, suggestion or motivation to use a ring structure in the gate area made of an insulating material.

19. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Mancevski by using a ring structure in the gate area made of an insulating material for advantages such as achieving a high-density integration in the final structure of the FET (Page 2, [0028]).

20. Also, a recitation of "wherein the first end portion of the nanostructure forms a first source/drain region and the second end portion of the nanostructure forms a second source/drain region of the field-effect transistor" of the claimed invention does not result in a structural difference between the claimed invention and the prior art, thus claimed invention is only an art recognized suitability for an intended purpose, MPEP 2144.07.

21. Furthermore, as for claim 43, it is obvious in view of the device disclose in Mancevski in view of Choi and claimed by the applicant since the claims only provide or form the different structures in the device, all of which are obvious by Mancevski in view of Choi.

22. As for claim 23, Mancevski discloses (Page 3 [0041]) that the catalyst (54) is deposit in the inner walls of the hole that start at the contact plane on the bottom

(applicant's limitation of catalyst material between the first conductive layer and the nanostructure).

23. As for claims 24 – 25, Mancevski shows in Fig. 2 that the third conductive layer/contact layer (20) surrounds the nanostructure in the middle of the transistor as well as it been thinner than both dielectric layer/spacing layers.

24. As for claim 27, Mancevski discloses the claimed invention except for the additional electrically conductive layer and ring structure in the structure. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to add the additional electrically conductive layer and ring structure in the structure, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

25. As for claim 28, Mancevski shows in Fig. 2 that creation of a second transistor (12) next to the original transistor (10).

26. As for claims 30 – 32, Mancevski discloses (Page 6 [0068]) that the structure is made out of doped silicon and metal films. Mancevski discloses the claimed invention except for the use of silicon dioxide, silicon nitride, or silicon dioxide doped with potassium ions for the dielectric material, the use of polysilicon, tantalum, titanium, niobium, or aluminum for the third and additional electrically conductive layer, and the use of tantalum, tantalum nitride, titanium, molybdenum, aluminum, titanium nitride, or ferromagnetic material as the first and second electrically conductive layer. It would have been obvious to one having ordinary skill in the art at the time of the invention was

made to use of silicon dioxide, silicon nitride, or silicon dioxide doped with potassium ions for the dielectric material, the use of polysilicon, tantalum, titanium, niobium, or aluminum for the third and additional electrically conductive layer, and the use of tantalum, tantalum nitride, titanium, molybdenum, aluminum, titanium nitride, or ferromagnetic material as the first and second electrically conductive layer, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

27. As for claims 33 - 36, Mancevski discloses (Page 3 [0040], Page 8 [0092]) the nanostructure been a carbon nanotube and the catalyst been Fe, Ni, or Co.

28. As for claim 37, it is an obvious variation of creating the nanostructure and the catalyst needed for that type of material.

29. If applicants disagrees, a restriction requirement might be then in order.

30. As for claim 38, Mancevski discloses (Page 2 – 3 [0022]) the use of a insulating material where the nanostructure is present starting from where it is formed all the way through the hole (applicant's limitation of via hole been filled by an electrically insulating spacer.

31. As for claims 39 – 40, Mancevski discloses (Page 6 [0068]) that the structure is made out of doped silicon and metal films (applicant's limitation of the structure been dielectric material, metallic material, and the nanostructure and the limitation of made of polycrystalline or amorphous material.

32. Claim 29 rejected under 35 U.S.C. 103(a) as being unpatentable over Mancevski in view of Martin et al. US 2001/0019279 (Martin).

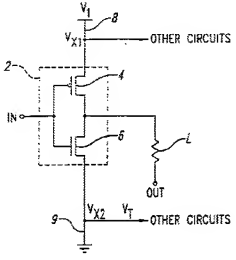


Fig. 1

33. As for claim 29, Mancevski discloses the claimed invention except for the use of the transistors as an inverter circuit. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to connect both transistors as a inverter circuit since it was known in the art that, as evidence in Martin, that the inviter circuit (2) takes the use of two transistors (4,6) connected as in Fig. 1 above. Furthermore, It would have been an obvious matter of intended use to connect both transistors as an inverter circuit, since applicant has not disclosed that this connection solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well in any other circuit with the need of two transistors. Finally, a recitation of "as an inverter circuit" of the claimed invention does not result in a structural difference between the claimed invention and the prior art, thus claimed invention is only an art-recognized suitability for an intended purpose, MPEP 2144.07.

Response to Arguments

34. Applicant's arguments with respect to claims 22 – 25, 27 – 37 and 39 – 45 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

35. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 5,362,972, US 4,903,089, US 5,308,778, US 5,286,674, and US 5,398,200.

36. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANDRES LOPEZ ESQUERRA whose telephone number is (571)272-9753. The examiner can normally be reached on M - Th 6:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven H. Loke can be reached on (571) 272 - 1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Andrés López-Esquerra
Examiner
Art Unit 2818

ALE

/DAVID VU/
Examiner, Art Unit 2818